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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/677,560	10/01/2003	Michael Lee Workman	Pillar 716	3994

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EXAMINER	
PARK, ILWOO	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 06/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/677,560	WORKMAN ET AL.	
	Examiner	Art Unit	
	Ilwoo Park	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 22-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 22-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/9/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-7, 22, and 23 are amended and claims 24-31 are added in response to the last office action. Claims 1-7 and 22-31 are presented for examination.

Claim Objections

2. Claim 24 is objected to because of the following informalities: the phraseologies "the first and second control paths" in line 15 are inconsistent with "a first communication line" and "a second communication line". Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 1, 3-7, and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over El-Batal et al. [US 2003/0221061 A1] in view of Borsini et al. [US 2004/0117545 A1] in further view of Felton et al. [US 2004/0193791 A1].

As to claims 1 and 31, El-Batal et al teach a coupling circuit for a Serial ATA storage device, comprising:

a first Serial ATA controller-side transceiver [e.g., analog front end 601 of fig. 6 in a physical layer interface 760 of fig. 7A] receiving a first Serial ATA communication path;

a second Serial ATA controller-side transceiver [e.g., analog front end 601 of fig. 6 in a physical layer interface 761 of fig. 7A] receiving a second Serial ATA communication path;

a Serial ATA device-side transceiver [e.g., analog front end 601 of fig. 6 at the storage device 742 in order to transmit and receive serialized datastream to and from the physical layer interfaces at the controllers side; disks are Serial ATA disks which are inputting and outputting serialized datastream in accordance with a Serial ATA Specification in paragraph 0051]; and

coupling circuit switches [e.g., multiplexer 741] which selectively coupling either the first Serial ATA controller-side transceiver or the second Serial ATA controller-side transceiver to the Serial ATA device-side transceiver based on the logic state of a path control line.

However, El-Batal et al do not expressly disclose the coupling circuit connected to storage device power through a power switch, connected to a first storage controller through a first communication line and connected to a second storage controller through a second bidirectional communication line and a microcontroller in the coupling circuit coupled to the coupling circuit switches and the power switch and adapted to control the coupling circuit switches and the power switch based on communication through the first or the second bidirectional communication lines. Borsini et al teach a coupling circuit for a Serial ATA storage device connected to storage device power through a power switch, connected to a first storage controller [e.g., BRIDGE CONTROL CARD A (ATA BCC A) 92 in fig. 3] through a first communication line [e.g., REQ_A_N, GNT_A_N

94, signal line 98 from ATA BCC A 92] and connected to a second storage controller [e.g., BRIDGE CONTROL CARD B (ATA BCC B) 92' in fig. 3] through a second bidirectional communication line [e.g., REQ_B_N, GNT_B_N 94', signal line 98 from ATA BCC B 92'] and a microcontroller [microcontroller 104 in fig. 4] in the coupling circuit coupled to the coupling circuit switches and the power switch and adapted to control the coupling circuit switches [paragraphs 0027, 0029] and the power switch [paragraphs 0027, 0030] based on communication through the first or the second bidirectional communication lines. At the time the invention, one of ordinary skill in the art would have been motivated to combine the cited disclosures in order to allow feasibility of Serial ATA communication path control between the two controllers and a Serial ATA disk and in order to allow feasibility of replacing the storage device due to failure [Borsini et al: paragraph 0007].

The combination of El-Batal et al and Borsini et al fails to specify that the bidirectional communication line are serial lines. Felton et al teach a coupling circuit having a microcontroller [e.g., microcontroller 300 in fig. 4] for controlling a power switch based on communication through a first bidirectional serial communication line from a first storage controller or a second bidirectional serial communication line [I^2C bus] from a second storage controller [paragraph 0065]. At the time the invention, one of ordinary skill in the art would have been motivated to modify the combination of references (El-Batal et al and Borsini et al) in order to reduce communication lines by having the serial lines as taught by Felton et al.

5. As to claim 3, Borsini et al teach the microcontroller includes a processor coupled to the power switch and coupled to the coupling switches [paragraphs 0027, 0029, 0030].

6. As to claim 4, El-Batal et al, Borsini et al, and Felton et al teach the microcontroller includes a processor coupled to a power switch and coupled to the coupling circuit switches; however, El-Batal et al, Borsini et al, and Felton et al do not disclose a set of logics including a set of D flip-flops. It is well known in the art that a set of logics including a set of D flip-flops for simplicity in order to latch a control signal from the microcontroller to simply eliminate burden of the microcontroller maintaining the control signal at the same level until next path change.

7. As to claim 5, Borsini et al teach the microcontroller is programmed to as follows: switch the coupling circuit to a first storage controller; switch the coupling circuit to a second storage controller; power up the Serial ATA storage device; and power down the Serial ATA storage device [paragraphs 0027-0030].

8. As to claim 6, Borsini et al teach the microcontroller further programmed to as follows: write data to a memory; read data from the memory; and read the status of the coupling circuit [paragraphs 0028, 0030; fig. 6].

9. As to claim 7, Borsini et al teach the status includes information on whether the storage is coupled to the first controller-side or the second controller-side, the storage is powered up or down, the communication status, and/or the board revision and code revision levels of the coupling circuit [paragraphs 0028, 0030; fig. 6].

10. Claim 22-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over El-Batal et al. [US 2003/0221061 A1] in view of Borsini et al. [US 2004/0117545 A1].

As to claim 22, El-Batal et al teach each of a plurality of coupling circuits for a single ported storage device comprising:

a first controller-side transceiver [e.g., analog front end 601 of fig. 6 in a physical layer interface 760 of fig. 7A] receiving a first communication path;

a second controller-side transceiver [e.g., analog front end 601 of fig. 6 in a physical layer interface 761 of fig. 7A] receiving a second communication path;

a storage device-side transceiver [e.g., analog front end 601 of fig. 6 at the storage device 742 in order to transmit and receive serialized datastream to and from the physical layer interfaces at the controllers side; disks are Serial ATA disks which are inputting and outputting serialized datastream in accordance with a Serial ATA Specification in paragraph 0051]; and

coupling circuit switches [e.g., multiplexer 741] which selectively coupling either the first controller-side transceiver or the second controller-side transceiver to the storage device-side transceiver based on the logic state of a path control line.

However, El-Batal et al do not expressly disclose the coupling circuit connected to storage device power through a power switch and a microcontroller coupled to the coupling circuit switches, the power switch, and a first and a second control paths, and adapted to control the coupling circuit switches and the power switch to the single ported storage device based on communication through the first or the second control paths. Borsini et al teach a coupling circuit for a single ported storage device connected

to storage device power through a power switch, connected to a first storage controller [e.g., BRIDGE CONTROL CARD A (ATA BCC A) 92 in fig. 3] through a first control path [e.g., REQ_A_N, GNT_A_N 94, signal line 98 from ATA BCC A 92] separate from a first communication path and connected to a second storage controller [e.g., BRIDGE CONTROL CARD B (ATA BCC B) 92' in fig. 3] through a second control path [e.g., REQ_B_N, GNT_B_N 94', signal line 98 from ATA BCC B 92'] separate from a second communication path and a microcontroller [microcontroller 104 in fig. 4] coupled to the coupling circuit switches, the power switch, and the first and the second control paths, and the power switch and adapted to control the coupling circuit switches [paragraphs 0027, 0029] and the power switch [paragraphs 0027, 0030] based on communication through the first or the second control paths. At the time the invention, one of ordinary skill in the art would have been motivated to combine the cited disclosures in order to allow feasibility of a single ported storage device communication path control between the two controllers and a single ported storage device and in order to allow feasibility of replacing the storage device due to failure [Borsini et al: paragraph 0007].

11. As to claim 23, El-Batal et al teach a coupling circuit for a Serial ATA storage device comprising:

means for receiving a first Serial ATA communication path [e.g., 712 in fig. 7A] receiving a first communication path;

means for receiving a second Serial ATA communication path [e.g., 732 in fig. 7A] receiving a second communication path; and

means for coupling [e.g., multiplexer 741] either the first Serial ATA communication path or the second Serial ATA communication path to the Serial ATA storage device.

However, El-Batal et al do not expressly disclose a microcontroller adapted to control the means for coupling and the power to the Serial ATA storage device based on inputs from communication lines outside the first and the second Serial ATA communication path. Borsini et al teach a microcontroller [microcontroller 104 in fig. 4] adapted to control the means for coupling [paragraphs 0027, 0029] and the power [paragraphs 0027, 0030] to the Serial ATA storage device based on inputs [e.g., REQ_A_N, GNT_A_N 94, signal line 98 from ATA BCC A 92 and REQ_B_N, GNT_B_N 94', signal line 98 from ATA BCC B 92'] from communication lines outside the first and the second Serial ATA communication path. At the time the invention, one of ordinary skill in the art would have been motivated to combine the cited disclosures in order to allow feasibility of a Serial ATA storage device communication path control between the two controllers and a Serial ATA storage device and in order to allow feasibility of replacing the storage device due to failure [Borsini et al: paragraph 0007].

12. As to claim 24, El-Batal et al teach a coupling circuit for a Serial ATA storage device, comprising:

a first Serial ATA controller-side transceiver [e.g., analog front end 601 of fig. 6 in a physical layer interface 760 of fig. 7A] receiving a first Serial ATA communication path;

a second Serial ATA controller-side transceiver [e.g., analog front end 601 of fig. 6 in a physical layer interface 761 of fig. 7A] receiving a second Serial ATA communication path;

a Serial ATA device-side transceiver [e.g., analog front end 601 of fig. 6 at the storage device 742 in order to transmit and receive serialized datastream to and from the physical layer interfaces at the controllers side; disks are Serial ATA disks which are inputting and outputting serialized datastream in accordance with a Serial ATA Specification in paragraph 0051]; and

coupling circuit switches [e.g., multiplexer 741] selectively coupling either the first Serial ATA controller-side transceiver or the second Serial ATA controller-side transceiver to the Serial ATA device-side transceiver based on the logic state of a path control line.

However, El-Batal et al do not expressly disclose the coupling circuit connected to storage device power through a power switch, and a microcontroller in the coupling circuit coupled to the coupling circuit switches, the power switch, and a first and a second control paths, and adapted to control the coupling circuit switches and the power switch based on communication through the first and the second communication lines. Borsini et al teach a coupling circuit for a Serial ATA storage device connected to storage device power through a power switch, connected to a first storage controller [e.g., BRIDGE CONTROL CARD A (ATA BCC A) 92 in fig. 3] through a first communication line [e.g., REQ_A_N, GNT_A_N 94, signal line 98 from ATA BCC A 92] separate from the Serial ATA communication paths and connected to a second storage

controller [e.g., BRIDGE CONTROL CARD B (ATA BCC B) 92' in fig. 3] through a second bidirectional communication line [e.g., REQ_B_N, GNT_B_N 94', signal line 98 from ATA BCC B 92'] separate from the Serial ATA communication paths and a microcontroller [microcontroller 104 in fig. 4] in the coupling circuit coupled to the coupling circuit switches, the power switch, and the first and second control paths, and the power switch and adapted to control the coupling circuit switches [paragraphs 0027, 0029] and the power switch [paragraphs 0027, 0030] based on communication through the first and the second communication lines. At the time the invention, one of ordinary skill in the art would have been motivated to combine the cited disclosures in order to allow feasibility of Serial ATA communication path control between the two controllers and a Serial ATA disk and in order to allow feasibility of replacing the storage device due to failure [Borsini et al: paragraph 0007].

13. As to claim 25, Borsini et al teach the microcontroller includes a processor coupled to the power switch and coupled to the coupling switches [paragraphs 0027, 0029, 0030].

14. As to claim 26, El-Batal et al, Borsini et al, and Felton et al teach the microcontroller includes a processor coupled to a power switch and coupled to the coupling circuit switches; however, El-Batal et al, Borsini et al, and Felton et al do not disclose a set of logics including a set of D flip-flops. It is well known in the art that a set of logics including a set of D flip-flops for simplicity in order to latch a control signal from the microcontroller to simply eliminate burden of the microcontroller maintaining the control signal at the same level until next path change.

15. As to claim 27, Borsini et al teach the microcontroller is programmed to as follows: power up the Serial ATA storage device; and power down the Serial ATA storage device [paragraphs 0027-0030].

16. As to claim 28, Borsini et al teach the microcontroller is programmed to as follows: switch the coupling circuit to a first storage controller; and switch the coupling circuit to a second storage controller [paragraphs 0027-0030].

17. As to claim 29, Borsini et al teach the microcontroller further programmed to as follows: write data to a memory; read data from the memory; and read the status of the coupling circuit [paragraphs 0028, 0030; fig. 6].

18. As to claim 30, Borsini et al teach the status includes information on whether the storage is coupled to the first controller-side or the second controller-side, the storage is powered up or down, the communication status, and/or the board revision and code revision levels of the coupling circuit [paragraphs 0028, 0030; fig. 6].

19. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over El-Batal et al., Borsini et al., and Felton et al. as applied to claim 1 above, and further in view of Deyring et al., US patent application publication No. US 2003/0158991 A1.

As to claim 2, El-Batal et al, Borsini et al, and Felton et al teach a Serial ATA Specification [in Physical Layer Section; paragraph 0005 of El-Batal et al] requires Out Of Band (OOB) signals need to be sent and received at each transceivers in order to detect COMRESET, COMINIT, and COMWAKE during a Serial ATA bus operation. However, El-Batal et al, Borsini et al, and Felton et al do not expressly disclose activating the first Serial ATA controller-side transceiver, the second Serial ATA

controller-side transceiver, and the Serial ATA storage device-side transceiver. Deyring et al teach an out of band squelch control component sending and receiving Out Of Band (OOB) signals sent and received at a transceiver by activating [figs. 1 and 5] the transceiver for a Serial ATA bus operation; and Deyring et al further teach [paragraph 0004] each transceiver is required at each end of the Serial ATA bus. Therefore, it would have been obvious to one of ordinary skill in the art of a Serial ATA bus operation at the time the invention was made to combine the teachings of El-Batal et al, Borsini et al, and Felton et al, and Deyring et al because they both teach a Serial ATA bus operation according to Serial ATA Specification and the Deyring et al's teaching of an out of band squelch control component activating each transceiver in order to send and receive OOB signals for a bus synchronization would increase reliability of El-Batal et al, Borsini et al, and Felton et al's Serial ATA bus operation.

Conclusion

20. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ilwoo Park whose telephone number is (571) 272-4155. The examiner can normally be reached on Monday through Friday from 9:00 AM to 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ILWOO PARK
PRIMARY EXAMINER

Ilwoo Park
June 19, 2006